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PATENT
5681-62001/SUN030050

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/766,698

Filed: January 28, 2004

Inventors:
Wallin, et al.

Title: COMPUTER SYSTEM EMPLOYING BUNDLED PREFETCHING

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Examiner: Unknown
Group/Art Unit: 2186
Atty. Dkt. No.: 5681-62001

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Rory D. Rankin
Printed Name

Signature

3/28/06
Date

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3. A copy of references A1 – A28 listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

a.
- ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
- ☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
- ☒ before the mailing date of a first Office Action on the merits; or
- ☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in § 1.56(c) more than thirty (30) days prior to the filing of the information disclosure statement;

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of the Statement; or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three (3) months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5681-62001/RDR.

Respectfully submitted,

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Date: 3/28/06

PTO/SB/08A (07-05)
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Substitute for form 1449/PTO Modified	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	Application Number	10/766,698
	Confirmation No.:	2084
	Filing Date:	January 28, 2004
	First Named Inventor:	Wallin, et al.
	Art Unit:	2186
	Examiner Name:	Unknown
Sheet 1 of 4	Attorney Docket Number:	5681-62001

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code-Number-Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	Check if English Translation is attached
						☐
						☐

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
	A1	ANANT AGARWAL, JOHN HENNESSY, and MARK HOROWITZ; Cache Performance of Operating System and Multiprogramming Workloads; Transactions on Computer Systems (TOCS); 1988; Vol. 6, No. 4; pps 393 – 431.	☐
	A2	ALAN CHARLESWORTH; The Sun Fireplane System Interconnect; 2001 Conference on Supercomputing; 2001; 14 pages; Denver CO, U.S.A.	☐
	A3	TIEN-FU CHEN and JEAN-LOUP BAER; A Performance Study of Software and Hardware Data Prefetching Schemes; International Symposium on Computer Architecture; 1994; pps 223 – 232.	☐
	A4	FREDRIK DAHLGREN, MICHEL DUBOIS and PER STENSTROM; Sequential Hardware Prefetching in Shared-Memory Multiprocessors; IEEE Transactions on Parallel and Distributed Systems; 1995; Vol. 6 No. 7; pps 733 – 746.	☐
	A5	FREDRIK DAHLGREN and PER STENSTROM; Evaluation of Hardware-Based Stride and Sequential Prefetching in Shared-Memory Multiprocessors; IEEE Transactions on Parallel and Distributed Systems; 1996; Vol. 7, No. 4; pps 385 – 398.	☐
	A6	MICHEL DUBOIS, JONAS SKEPPSTEDT, LIVIO RICCIULLI, KRISHNAN RAMAMURTHY, and PER STENSTROM; The Detection and Elimination of Useless Misses in Multiprocessors; International Symposium on Computer Architecture; 1993; pps 88 – 97.	☐

PTO/SB/08A (07-05)
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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application. [1]Applicant's unique citation designation number (optional).

Substitute for form 1449/PTO Modified	*Complete if Known*	
INFORMATION DISCLOSURE **STATEMENT BY APPLICANT** ***(Use as many sheets as necessary)*** Sheet 2 Of 4	Application Number Confirmation No.: Filing Date: First Named Inventor: Art Unit: Examiner Name: Attorney Docket Number:	10/766,698 2084 January 28, 2004 Wallin, et al. 2186 Unknown 5681-62001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
	A7	SUSAN J. EGGERS and TOR E. JEREMIASSEN; Eliminating False Sharing. 1991 International Conference on Parallel Processing; 1991; pps 377 – 381.	☐
	A8	SUSAN J. EGGERS and RANDY H. KATZ; The Effect of Sharing on the Cache and Bus Performance of Parallel Programs. International Conference on Architectural Support for Programming Languages and Operating Systems; 1989; pps 257 – 270.	☐
	A9	FREDRIK DAHLGREN and PER STENSTROM; Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors; IEEE Transactions on Computers; 1998; Vol. 47, No. 10; pps 1041 – 1055.	☐
	A10	M. J. GARZARAN, J. L. BRIZ, P. E. IBANEZ, and V. VINALS; Hardware Prefetching in Bus-Based Multiprocessors: Pattern Characterization and Cost-Effective Hardware; Parallel and Distributed Processing; 2001, pages 345 – 354.	☐
	A11	JAMES R. GOODMAN; Using Cache Memory to Reduce Processor-Memory Traffic; In 25 Years of the International Symposia on Computer Architecture (selected papers); 1998; pps 255 – 262.	☐
	A12	ANOOP GUPTA and WOLF-DIETRICH WEBER; Cache Invalidation Patterns in Shared-Memory Multiprocessors. IEEE Transactions on Computers; 1992; Vol. 41, No. 7; pps 794 – 810.	☐
	A13	MARTIN KARLSSON, KEVIN MOORE, ERIK HAGERSTEN, and DAVID A. WOOD; Memory System Behavior of Java-Based Middleware; Ninth Annual International Symposium on High-Performance Computer Architecture (HPCA-9); 2003; 12 pages.	☐
	A14	DAVID M. KOPPELMAN; Neighborhood Prefetching on Multiprocessors Using Instruction History; International Conference on Parallel Architectures and Compilation Techniques; 2000; pps 123 – 132.	☐
	A15	SANJEEV KUMAR and CHRISTOPHER WILKERSON; Exploiting Spatial Locality in Data Caches using Spatial Footprints; International Symposium on Computer Architecture; 1998; pps 357 – 368.	☐
	A16	PETER S. MAGNUSSON, MAGNUS CHRISTENSSON, JESPER ESKILSON, DANIEL FORSGREN, GUSTAV HALLBERG, JOHAN HOGBERG, FREDRIK LARSSON, ANDREAS MOESTEDT, and BENGT WERNER; Simics: A Full System Simulation Platform; IEEE Computer, 2002; Vol. 35 No. 2; pps 50 – 58.	☐

Examiner Signature		Date Considered	

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	Confirmation No.:	2084
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	First Named Inventor:	Wallin, et al.
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Sheet 3 Of 4	Attorney Docket Number:	5681-62001

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	A17	TODD MOWRY and ANOOP GUPTA; Tolerating Latency Through Software-Controlled Prefetching in Shared-Memory Multiprocessors; Journal of Parallel and Distributed Computing; 1991; Vol. 12, No. 2; pps 87 – 106.	☐
	A18	TODD C. MOWRY; Tolerating Latency in Multiprocessors through Compiler-Inserted Prefetching. Transactions on Computer Systems (TOCS); 1998; Vol. 16, No. 1; pps 55 – 92.	☐
	A19	STEVEN PRZYBYLSKI; The Performance Impact of Block Sizes and Fetch Strategies; International Symposium on Computer Architecture; 1990; pps 160 – 169.	☐
	A20	ANDRE SEZNEC; Decoupled Sectored Caches: conciliating low tag implementation cost and low miss ratio; 21st Annual International Symposium on Computer Architecture; 1994; pps 384 – 393.	☐
	A21	JOSEP TORRELLAS, MONICA S. LAM, and JOHN L. HENNESSY; False Sharing and Spatial Locality in Multiprocessor Caches; IEEE Transactions on Computers; 1994; Vol. 43, No. 6; pps 651 – 663.	☐
	A22	DEAN M. TULLSEN and SUSAN J. EGGERS; Effective Cache Prefetching on Bus-Based Multiprocessors; Transactions on Computer Systems (TOCS); 1995; Vol. 13, No. 1; pps 57 – 88.	☐
	A23	DEAN M. TULLSEN and SUSAN J. EGGERS; Limitations of Cache Prefetching on Bus-Based Multiprocessor; 20th Annual International Symposium on Computer Architecture; 1993; pps 278 - 288.	☐
	A24	STEVEN CAMERON WOO, MORIYOSHI OHARA, EVAN TORRIE, JASWINDER PAL SINGH, and ANOOP GUPTA; The SPLASH-2 Programs: Characterization and Methodological Considerations; 22nd Annual International Symposium on Computer Architecture; 1995; pps 24 – 36.	☐
	A25	ALEXANDER V. VEIDENBAUM, WEIYU TANG, and RAJESH GUPTA; "Adapting Cache Line Size to Application Behavior"; In Proceedings of the 13th International Conference on Supercomputing; 1999; pps 145 – 154.	☐
	A26	http://ecperf.theserverside.com/ecperf/; The publication date of this internet web page predates the filing date of the current application.	☐
	A27	http://www.spec.org/jAppServer2001/press_release.html; The publication date of this internet web page predates the filing date of the current application.	☐
	A28	http://www.spec.org/jbb2000/; The publication date of this internet web page predates the filing date of the current application.	☐
	A29	TIEN-FU CHEN and JEAN-LOUP BAER; An Effective On-Chip Preloading Scheme to Reduce Data Access Penalty; In Proceedings of Supercomputing, 1991; pps176 – 186.	

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NON PATENT LITERATURE DOCUMENTS			
	A30	EDWARD H. GORNISH; Adaptive and Integrated Data Cache Prefecting For Shared-Memory Multiprocessors; PhD thesis, University of Illinois at Urbana-Champaign; 1995; pps1-150	☐
	A31	ERIK HAGERSTEN; Toward Scalable Cache-Only Memory Architectures; PhD thesis, Royal Institute of Technology, Stockholm; 1992; pps1-262	☐
	A32	ASHOK SINGHAL et al.; A High Performance Bus for Large SMPs; In Proceedings of IEEE Hot Interconnects; 1996	☐
	A33	M.K. TCHEUN, H. YOON, and S.R. MAENG; An Adaptive Sequential Prefetching Sequential Prefetching Scheme in Shared-Memory Multiprocessors; Department of Computer Science and Technology (KAIST); 1997; pps306-313	☐
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